Flexible memory device based on polymer ferroelectric with zinc oxide single-nanowire transistors for robust multilevel operation

Young Tea Chun [a,b], Jiyoul Lee [c,d,*], Daping Chu [a,**]

[a] *Electrical Engineering Division, Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom*

[b] *Division of Electrics and Electrical Information Engineering, Korea Maritime & Ocean University, 727 Taejong-ro, Yeongdo-gu, Busan, 49112, Republic of Korea*

[c] *Department of Nanotechnology Engineering, Pukyong National University, 45 Yongso-ro, Nam-gu, Busan 48513, Republic of Korea*

[d] *Department of Smart Green Technology Engineering, Pukyong National University, 45 Yongso-ro, Nam-gu, Busan 48513, Republic of Korea*

ABSTRACT

We demonstrate a flexible ferroelectric polymer-based memory with a zinc oxide (ZnO) single-nanowire transistor; its enhanced memory properties are attributed to the limited size of the semiconducting single-nanowire, which suppresses leakage currents caused by parasitic capacitance. Memory devices based on hybrid ferroelectric field-effect transistors (Fe-FETs) exhibit an outstanding data retention time, with an on/off ratio of ~10^7 for 10^4 s along with a highly stable endurance for 100 cycles, without drain current degradation at a readout voltage of 0.1 V. Furthermore, these enhanced characteristics lead to a robust performance, overcoming the changes in the hysteresis window caused by flexoelectricity under bending stress; thus, the flexible-polymer Fe-FET with a ZnO single-nanowire channel shows a multilevel switching behavior with three different drain current states under bending conditions.

KEYWORDS: ferroelectric copolymer, ZnO single-nanowire , flexible memory device, synaptic neural device, flexoelectricity.

* Author to whom correspondence should be addressed. Electronic mail: jiyoul_lee@pknu.ac.kr (J. L.)
** Author to whom correspondence should be addressed. Electronic mail: dpc31@cam.ac.uk (D. C.)

The increasing popularity of exascale computing applications such as big data analytics has resulted in greater technical demands for high-performance computing systems capable of faster and more efficient data processing.[1] Neuromorphic systems, which efficiently process information by emulating the function of the human brain, are considered promising technologies to meet these demands.[2,3] The human brain uses a complex neural network composed of neurons and synapses to simultaneously process and store data in the same unit; in this way, it can process information efficiently while consuming very low energy.[2-6] Pioneering attempts to mimic the ability of the brain to efficiently process and store information at same time involved extensive research on ferroelectric synaptic weights for artificial neural networks.[3-6] Ferroelectric synaptic neuron devices, serving as basic units for neuromorphic computing by generating a pulse that activates a new input, have been obtained through a multilevel operation in ferroelectric field-effect transistors (Fe-FETs) memory devices.[6,7]

Meanwhile, with the emergence of portable electronic devices such as smart glasses, watches, and wristbands, flexible electronics have recently attracted broad research interest. This is because it can be operated while changing their shape, and thus have excellent portability.[8] Therefore, integrating neuromorphic devices into flexible electronics is expected to support new electronic applications.[9] However, generally, inorganic-based ferroelectric materials with high-performance memory properties are mechanically brittle, and special fabrication processes are required to make them flexible. At the same time, ferroelectric polymer materials with intrinsic mechanical flexibility, such as poly(vinylidenefluoride-*co*-trifluoroethylene) [P(VDF-TrFE)], can be fabricated on flexible substrates by solution processing, but show inferior memory performance compared to their inorganic counterparts.[10-13] Given clear advantages and disadvantages of each ferroelectric material, we selected the P(VDF-TrFE) ferroelectric copolymer, which exhibits

superior properties in terms of mechanical flexibility and device fabrication. To compensate for the inferior memory properties while maintaining the advantages associated with the ferroelectric copolymer, we used a zinc oxide (ZnO) single-nanowire as the channel of the Fe-FET; with this design, the limited size of the single-nanowire should suppress the leakage current caused by parasitic capacitance. A polymeric Fe-FET memory incorporating the ZnO single-nanowire transistor was fabricated on a polyethylene terephthalate (PET) substrate in a low-temperature process (reaching a maximum of 150 °C). The device exhibited a wide memory window, an on/off current ratio higher than 10^7, and outstanding data retention characteristics for 10^4 s under a readout voltage of 0.1 V. In addition, the Fe-FET device showed stable memory properties under both tensile and compressive bending conditions. More importantly, these stable memory characteristics enable the flexible Fe-FET memory devices to achieve multilevel weight-control operation with three different current states under bending conditions, which is critical for their application in flexible neuromorphic systems.

ZnO nanowires were grown by chemical vapor deposition (CVD) in a tube furnace. A 1.5 nm Au layer was evaporated by an e-beam evaporator for catalyst on an oxidized (300 nm) Si (111) substrate. The prepared substrate was placed in an alumina boat on top of a 1:1 mixture of ZnO powder and carbon nanopowders, after which the alumina boat was positioned in the center of the furnace. The growth temperature of the mullite work tube was increased to 950 °C at a heating rate of 15 °C/min, while a 1:25 mixture of oxygen and argon gases was introduced to allow oxidation of the ZnO powders. When the growth temperature reached 950 °C, the melted zinc clusters were transferred to the Si substrate by the mixture gas flow stream. After that, the furnace was cooled down to room temperature and gray-colored ZnO nanowires were formed on the top of the Si substrate. The as-grown ZnO nanowires were characterized by SEM and high-resolution

TEM. A 5 wt.% P(VDF-TrFE) ferroelectric copolymer was prepared by dissolving P(VDF-TrFE) powder (70:30 molar ratio, Piezotech) in cyclohexanone (Sigma-Aldrich) at a concentration of 46 mg/mL stirring at 50 °C for 24 h, to melt in air ambient without any further filtering. The flexible Fe-FET memory was fabricated on a PET substrate. The grown ZnO nanowires were dispersed on a cleaned PET substrate. Source/drain (Ti/Au) electrodes of 70 nm/130 nm thicknesses were deposited by an e-beam evaporator under a vacuum of ~10^{-7} torr and patterned *via* photolithography. The prepared ferroelectric copolymer was spin-coated at 1,500 rpm for 1 min and dried on a hot plate at 150 °C in air ambient for 4 h. To complete the device fabrication, a 100 nm-thick Al top-gate electrode was deposited through a shadow mask by an e-beam evaporator in a vacuum of ~ 10^{-7} torr. The electrical characteristics of the devices were measured with Keithley 4200 and Agilent 4156C semiconductor parameter analyzers using a probe station located in a dark box. The mechanical flexibility of the flexible Fe-FET memory was investigated using lab-made bending devices, with the same bending radius (5.75 mm) for both tensile and compressive modes.

Before fabricating flexible Fe-FET devices, we investigated the electrical properties of the ZnO single-nanowire to be used as the channel of the flexible Fe-FET. The scanning electron microscopy (SEM) image in **Figure 1**(a) shows that the ZnO nanowires grew uniformly and vertically on the entire silicon substrate. Their diameters and lengths ranged from 100 to 130 nm and from 8 to 13 μm, respectively. The selective-area electron diffraction (SAED) pattern of ZnO single-nanowire in the inset of Figure 1(a) shows high-crystallinity diffraction spots. The high-resolution transmission electron microscopy (TEM) image in the Figure S1 of the supplementary material shows that the ZnO nanowires had high crystalline quality, with no dislocations or stacking of lattice fringes and consistent growth along the c-axis. The image clearly shows a lattice

spacing of 0.52 nm along the [0001] axis. The superior quality of these nanowires was reflected in the electrical performance of a ZnO single-nanowire-based transistor fabricated with a 200 nm-thick SiO_2 insulator. Figure 1(b) shows the transfer characteristics (I_{DS}–V_{GS}) and the V_{GS}-dependent electron mobility values of the ZnO single-nanowire TFT at a relatively small drain voltage (V_{DS}) of 0.1 V, chosen to minimize the effect of the lateral electric-field. The device showed a maximum current of 0.37 μA at a gate voltage (V_G) of 20 V, along with an on/off current ratio > 10^7 and a subthreshold swing (*SS*) of 0.5 V/decade. The linear mobility (μ_{linear}) was calculated using the following equation:[14,15]

$$\mu_{linear} = \frac{g_m}{C_{ins} V_{DS} \frac{W}{L}} \quad (1)$$

where L is the channel length, C_{ins} is the capacitance per unit area of the insulator, V_{DS} = 0.1 V, and g_m is the transconductance ($\partial I_{DS}/\partial V_{GS}$) of the transistor. The gate capacitance of the nanowire transistor is different from that of a typical TFT (with planar geometry); therefore, in this study it was calculated using the cylinder-on-an-infinite-metal-plate model:[16-18]

$$C_{ins} = \frac{2\pi\varepsilon_o\varepsilon_r L}{cosh^{-1}(1+\frac{t}{r})} \quad (2)$$

where r is the nanowire radius (50 nm), L = 4 μm, ε_o is the permittivity constant of vacuum, ε_r is the dielectric constant of SiO_2 (i.e., 3.9), and t is the thickness of the insulator (200 nm). The maximum linear mobility of the ZnO single-nanowire TFT was calculated to be 164.76 cm^2/Vs. Figure 1(c) shows the output characteristics of the ZnO single-nanowire TFT. The linear sections of the output curves near V_{DS} = 0 V indicate a good ohmic contact between the nanowire and the drain/source electrodes. This is attributed to relatively low Schottky barriers at the interface

between the electrode (Ti/Au; effective work function, ϕ_{Ti} = 4.33 eV) and the ZnO nanowire, which had an electron affinity (χ_{ZnO}) of 4.29 eV and a work function (ϕ_{ZnO}) of 4.45 eV.[19]

Figures 2(a) and (b) show a 3D scheme of the device structure used in this study and a photograph of the Fe-FET memory devices fabricated on a flexible substrate, respectively. Flexible Fe-FET memory devices were constructed with a top-gate structure consisting of a ZnO single-nanowire channel, a source/drain (Ti/Au) electrode, and a P(VDF-TrFE) ferroelectric copolymer layer. The thickness of the P(VDF-TrFE) layer was 270 nm, while the channel length was 4 μm; the ZnO nanowire was ~13 μm long with a diameter of ~130 nm. Figure 2(c) shows hysteresis loops of the flexible Fe-FET as a function of V_G, which were used for determining the transfer characteristics at V_{DS} = 0.1 V and a scan rate of 0.3 V/s. The Fe-FET showed a high on-current of 0.38 μA at V_G = 30 V and an outstanding on/off current ratios of more than 10^6 at V_{DS} = 0.1 V. The transfer curves show counterclockwise memory hysteresis loops originating from switching the alignment of the ferroelectric dipoles of the copolymer; the size of the loops gradually increased with the gate voltage sweeping range, and the maximum memory window was ~ 40 V at a V_G sweeping range of ±40 V, as shown in Figure 3(c). Electrical characterizations of the devices were performed with a gate voltage sweeping range of ±30 V, which provided a sufficient window to assess the memory. The reliability of the Fe-FET memory device was assessed using time-dependent data retention and endurance cycling tests between on and off states, performed at V_{DS} = 0.1 V for 10^4 s and 100 cycles. Figure 2(d) shows the data retention performance of the Fe-FET memory under a write voltage pulse V_G of ± 30 V for 2 s and a reading voltage V_G = 0 V for 10^4 s. Each gate voltage pulse aligned the dipole moments in the copolymer layer, and a corresponding accumulation or depletion of electrons occurred in the ZnO single-nanowire . In the on state, the current showed a slight increase until 1,500 s, after which the device reached a steady

state, while the off current remained stable at ~ 10^{-12} A. The Fe-FET memory assembled on a flexible substrate exhibited an outstanding on/off ratio of more than 5×10^5 for data retention over 10^4 s. Figure 2(e) shows the device endurance during 100 cycles of switching between on and off conductance states, along with a detailed view of the last 10 cycles; the current modulation was measured at V_{DS} = 0.1 V and V_{GS} = 0 V, as write and erase pulse voltages of ±30 V were applied for 3 s.

To evaluate the performances of the Fe-FET devices under mechanical deformation, their memory performances under tensile and compressive bending were assessed by examining the memory window, retention time, cycling endurance, and other properties. **Figures 3**(a–c) show the results of electrical measurements under compressive stress under a bending radius of 5.75 mm. The transfer curve was measured with V_G sweeping a range of ±30 V at V_{DS} = 0.1 V, and shows a counterclockwise ferroelectric hysteresis similar to that of the flat condition. Figure 3(b) shows the time evolution of the data retention for a readout voltage of 0.1 V. Importantly, the on/off ratio of the retention time test was ~ 10^7, which is 100 times higher than that of other inorganic nanowire-based Fe-FETs.[20-23] It is worth noting that this remarkably high on/off ratio is the most desirable characteristic for weight-control of ferroelectric synaptic neurons in neuromorphic systems. The ferroelectric effect was much stronger under compressive than tensile bending, and the memory window was significantly wider. The ferroelectric dipole charges therefore prevented degradation of the on-current, even in the presence of a leakage current; this is discussed in more detail below. Figure 3(c) shows that during writing endurance tests of 100 cycles, the flexible Fe-FET memory devices with the ZnO single-nanowire channel exhibited consistent and reliable performances under compressive stress, similar to those in unstressed conditions. Figures 4(d–f) show the results obtained for the flexible Fe-FET memory devices under tensile stress with a

bending radius of 5.75 mm. The time dependence of the on-currents for data retention and endurance cycling were reduced by almost one order of magnitude. However, the off-current level was similar to that measured before bending.

To further investigate the effect of a mechanical deformation applied to the flexible Fe-FET devices on their electrical and memory properties, the transfer curves under different bending conditions are compared in **Figure 4**(a). Compared with the flat, under compressive bending the flexible Fe-FET memory reached the off and on states at more negative and less positive voltages, respectively; thus, its memory window shifted in the negative direction and became wider, resulting in enhanced performances compared to the flat Fe-FET memory device. In contrast, under tensile bending, the device reached the off and on states at a less negative and more positive voltage, respectively; the memory window thus became slightly narrower and shifted in the positive direction, leading to relatively inferior memory performances. These changes in the memory properties can be explained in terms of flexoelectric effects: i.e., the generation of electric polarization under a strain gradient.

Under compressive bending, without any applied voltage, a downward-oriented polarization is generated by the strain gradient in the P(VDF-TrFE) layer. This ferroelectric copolymer has a permanent dipole perpendicular to the chain axis due to the negative fluorine and positive hydrogen atoms, and its polarization originates from a long-range alignment between the dipoles *via* rotation of the molecular chains. This spontaneous polarization creates an electrical field upon bending, which induces additional charges. As a consequence, the Fe-FET device is turned on at a lower voltage. Furthermore, as the preferential polarization under compressive bending is directed downward, the polarization reversal from the downward to the upward direction (which appears in Fe-FETs as a transition from the on to the off state) is hindered, as

shown in Figure 4(a). On the other hand, tensile bending conditions create an upward polarization, which shifts the memory window in the positive direction. However, the magnitude of the negative strain gradient along the copolymer chains is relatively small.[24,25] A second possible reason for the observed variation of the turn-on and turn-off voltages and for the shift in memory window is the piezoelectric effect, which in the present system would generate electrical charges at the interface between the single ZnO nanowire and the ferroelectric copolymer film.[26-27] Similar to flexoelectricity, the piezoelectric effect can induce additional charges and alter the turn-on and turn-off voltages as well as the memory window of the device under mechanical deformation. However, the piezoelectric effect would be dominant only if the ZnO nanowire is in contact with the ferroelectric copolymer. To determine the origin of the deformation-dependent memory properties of the Fe-FET memory device, the capacitance changes of metal–insulator–metal (MIM) device in which the copolymer film was sandwiched by metal electrodes on plastic substrates were measured under different bending conditions. The capacitance–voltage (C–V) curves of the MIM device [Figure 4(b)] show that not only the capacitance value but also the peak position (i.e., the voltage corresponding to the maximum capacitance value) changed according to the mechanical deformation. Moreover, the direction of the shift and the peak-to-peak width showed a clear correlation with the changes in the transfer curves due to mechanical deformation, shown in Figure 4(a). In other words, even though the MIM device included only a ferroelectric copolymer thin film (without any ZnO nanowire), its capacitance under mechanical deformation varied by ±10% in comparison with the peak value of the flat device. These results reveal that a change in the amount of polarization (rather than a generation of charges) took place in the ferroelectric copolymer film. Thus, it can be inferred that the flexoelectricity-induced polarization upon mechanical deformation was more dominant than the piezoelectricity-induced charge

generation. Figure 4(c) displays the three-level weight operation of the Fe-FET memory under a tensile bending radius of 5.75 mm. Two different I_{DS} values, depending on the gate-voltage (V_G = 30 V and V_G = 20 V), where observed at V_{DS} = 0.1 V. As discussed above, for the flexible Fe-FET memory, tensile bending conditions resulted in a degraded memory performance, owing to the negatively induced flexoelectric effect. However, despite the reduced on-current levels, stable multilevel weighting operation of the flexible Fe-FET memory is possible because integrating the high-quality ZnO single-nanowire into flexible Fe-FET memory minimizes leakage currents due to parasitic capacitance and keeps low off-current level.

In summary, we fabricated a flexible Fe-FET memory using high-quality ZnO single-nanowire with a very high mobility of 164.76 cm^2/V. Under both tensile and compressive stress bending conditions, the flexible Fe-FET memory exhibited a wide memory window of more than 40 V, excellent data retention with an on/off ratio of ~ 10^7 for 10^4 s at a low readout voltage of 0.1 V, and reliable endurance for 100 switching cycles without degradation. Moreover, regardless of the flexoelectric effect, the flexible Fe-FET memory showed stable multilevel weight-control with a high on/off ratio >10^5. The enhanced memory properties can be attributed to the confinement effect in the ZnO single-nanowire, which suppresses leakage currents due to parasitic capacitance.

See supplementary material for the HR-TEM image of ZnO nanowire and the surface and electrical properties of the P(VDF-TrFE) ferroelectric films

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] D. A. Reed, J. Dongarra, *Commun. ACM* **58 (7)**, 56 (2015).

[2] L. T. Clark, R. O. Grondin, S. K. Dey, *IC Neural Networks with Ferroelectric Capacitor Connections. First IEE Conf. on Artificial Neural Networks*, London, England; IEE Conference Publication **313**, 47 (1989).

[3] G. W. Burr, R.M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola, L. L. Sanches, I. Boybat, M. Le Gallo, K. Moon, J. Woo, H. Hwang, Y. Leblebici, *Adv. Phys. X*, **2(1)**, 89 (2017).

[4] D. Ielmini, H. S. P. Wong, *Nat. Electron*. **1**, 333 (2018).

[5] Q. Xia, J. J. Yang, *Nat. Mater*. **18**, 309 (2019).

[6] S. Oh, H. Hwang, I. K. Yoo, *APL Mater*. **7**, 091109 (2019).

[7] L. Liao, H. Fan, B. Yan, Z. Zhang, L. Chen, B. Li, G. Xing, Z. Shen, T. Wu and X. Sun, Acs Nano **3** (3), 700-706 (2009).

[8] K.-J. Baeg, J. Lee, *Adv. Mater. Tech*. **5**, 2000071 (2020).

[9] D. Kim, I.-J. Kim, J.-S. Lee, *Adv. Intell. Syst*. **3**, 2000206 (2021).

[10] L. W. Martin, A. M. Rappe, *Nat. Rev. Mater*. **2**, 16087, (2017).

[11] H. Sun, Z. Luo, L. Zhao, C. Liu, C. Ma, Y. Lin, G. Gao, Z. Chen, Z. Bao, X. Jin, Y. Yin, Li, X. Li, *ACS Appl. Electron. Mater.* **2**, 1081 (2020).

[12] R. C. Naber, K. Asadi, P. W. Blom, D. M. de Leeuw, B. de Boer, *Adv. Mater*. **22(9)**, 933 (2010).

[13] Y. T. Lee, P. J. Jeon, K. H. Lee, R. Ha, H. J. Choi, S. Im, *Adv. Mater.* **24(22),** 3020 (2012).

[14] C. -S. Li, Y.-N. Li, Y.-l. Wu, B.-S. Ong, R.-O. Loutfy, *Jour. Mater. Chem.* **19 (11)**, 1626 (2009).

[15] T. I. Suzuki, A. Ohtomo, A. Tsukazaki, F. Sato, J. Nishii, H. Ohno, M. Kawasaki, *Adv. Mater.* **16 (21)**, 1887 (2004).

[16] T. Kuykendall, P. Pauzauskie, S. Lee, Y. Zhang, J. Goldberger, P. Yang, *Nano Letters* **3(8)**, 1063 (2003).

[17] W. Wang, H. D. Xiong, M. D. Edelstein, D. Gundlach, J. S. Suehle, C. A. Richter, W.-K. Hong, T. Lee, *J. Appl. Phys.* **101(4)**, 044313 (2007).

[18] O. Wunnicke, *Appl. Phys. Lett.* **89 (8)**, 083102 (2006).

[19] S. Ju, S. Kim, S. Mohammadi, D. B. Janes, Y.-G. Ha, A. Facchetti, T. J. Marks, *Appl. Phys. Lett.* **92(2)**, 022104 (2008).

[20] S. J. Kang, I. Bae, Y. J. Park, T. H. Park, J. Sung, S. C. Yoon, K. H. Kim, D. H. Choi, C. Park, *Adv. Funct. Mater.* **19 (10)**, 1609 (2009).

[21] M. Khan, U. S. Bhansali, H. N. Alshareef, *Adv. Mater.* **24 (16)**, 2165 (2012).

[22] R. H. Kim, H. J. Kim, I. Bae, S. K. Hwang, D. B. Velusamy, S. M. Cho, K. Takaishi, T. Muto, D. Hashizume, M. Uchiyama, *Nat. comm.* **5 (1)**, 1 (2014).

[23] N. H. Van, J.-H. Lee, D. Whang, D. J. Kang, *Nanoscale* **7 (27)**, 11660 (2015).

[24] J. Liu, Y. Zhou, X. Hu, B. Chu, *Appl. Phys. Lett.* **112 (23)**, 232901 (2018).

[25] C. Wang, Y. Zhang, B. Zhang, B. Wang, J. Zhang, L. Q. Chen, Q. Zhang, Z. L. Wang, K. Ren, *Adv. Sci.* ***8*** **(8)**, 2004554 (2021).

[26] J. Li, C. Zhao, K. Xia, X. Liu, D. Li, J. Han, *Appl. Surf. Sci.* **463**, 626-634 (2019).

[27] A. Matsumoto, S. Horie, H. Yamada, K. Matsushige, S. Kuwajima, K. Ishida, *Appl. Phys. Lett.* **90 (20)**, 202906 (2007).

Figure 1.

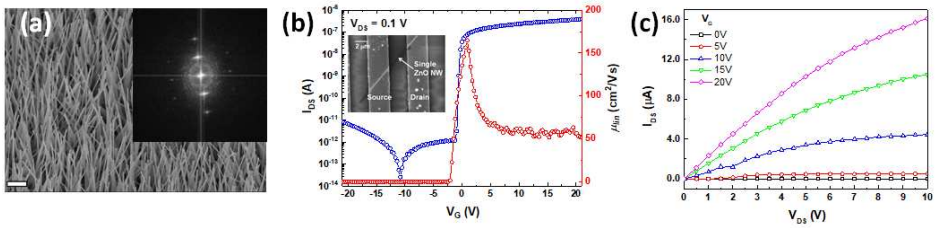

Figure 1. (a) SEM image of as-grown ZnO nanowires (scale bar, 2 μm). The inset shows a SAED pattern of the ZnO single-nanowire. (b) Plots of transfer characteristics and linear mobility *vs*. applied gate bias for ZnO single-nanowire transistor on SiO_2/*n*-Si substrate. The inset shows a SEM image of the transistor. (c) Output curves of ZnO single-nanowire transistor.

Figure 2.

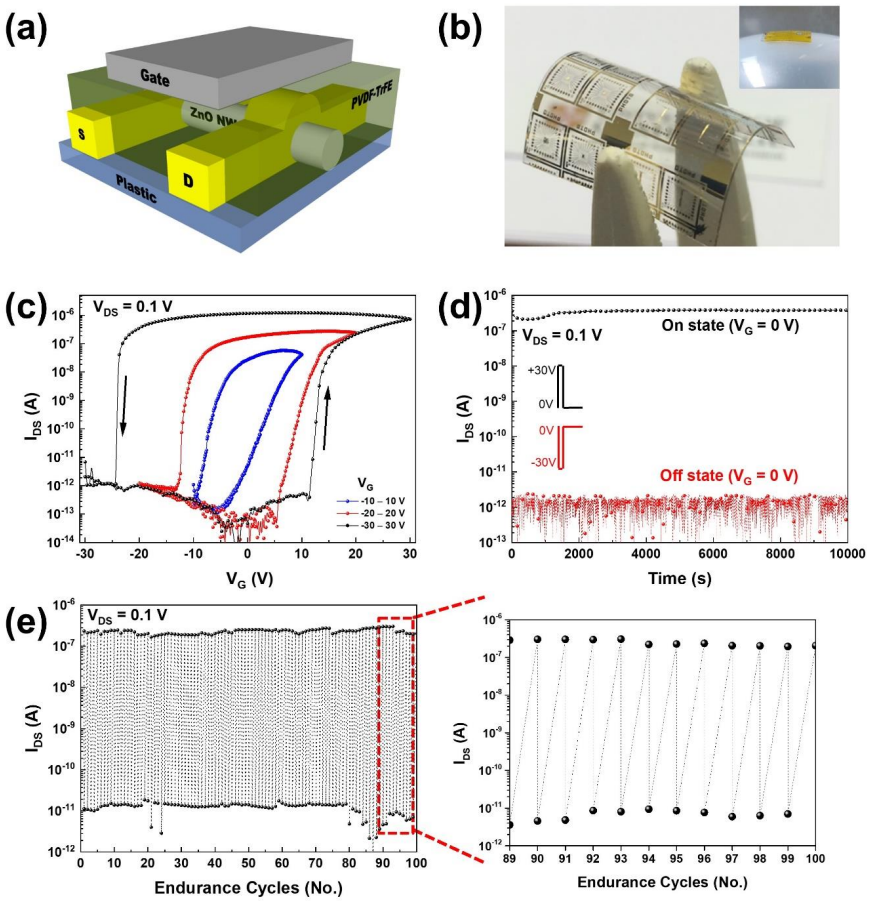

Figure 2. (a) 3D schematic illustration of polymer Fe-FET incorporating ZnO nanowire with top-gate structure. (b) Photograph of Fe-FET memory device fabricated on a flexible plastic substrate. The inset shows a photo of the Fe-FET memory devices on a sphere-shaped surface. (c) Transfer characteristics of Fe-FET measured with various gate voltage sweeping ranges (up to $-40\ \text{V} \leq V_G \leq +40\ \text{V}$) at $V_{DS} = 0.1$ V. (d) Data retention of on and off states at a readout voltage of 0.1 V for 10,000 s. (e) Programmed endurance tests covering 100 cycles between on and off states (left) and enlarged view of the last 10 cycles (right).

Figure 3.

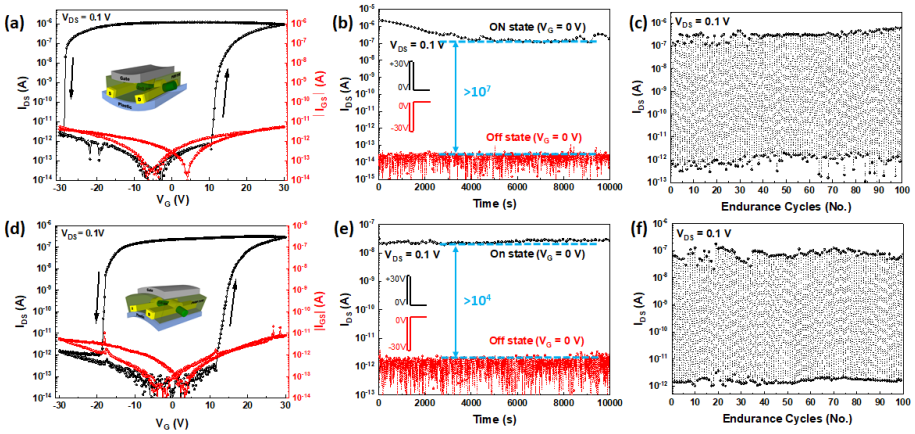

Figure 3. Memory properties of flexible Fe-FET memory device under (a)–(c) compressive bending (radius 5.75 mm) and (d)–(f) tensile bending (radius 5.75 mm).

Figure 4.

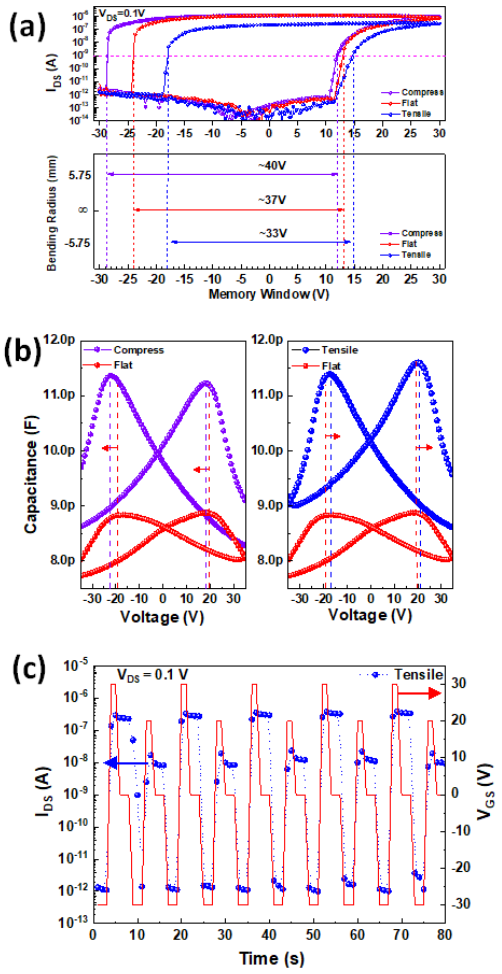

Figure 4. (a) Transfer curves under different bending conditions (top) and corresponding changes in memory window (bottom) of the Fe-FET devices. (b) *C–V* characteristics of a MIM device with a copolymer film sandwiched between electrodes, measured at 1 MHz under different bending conditions. (c) Three-level memory operation of Fe-FET device under tensile bending conditions.

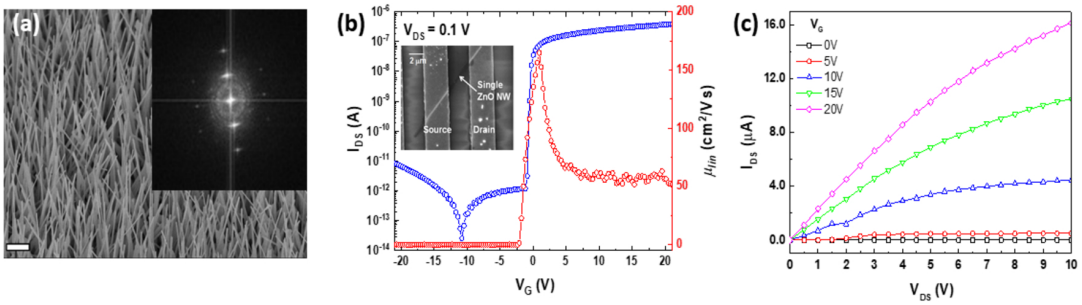

Figure 1.

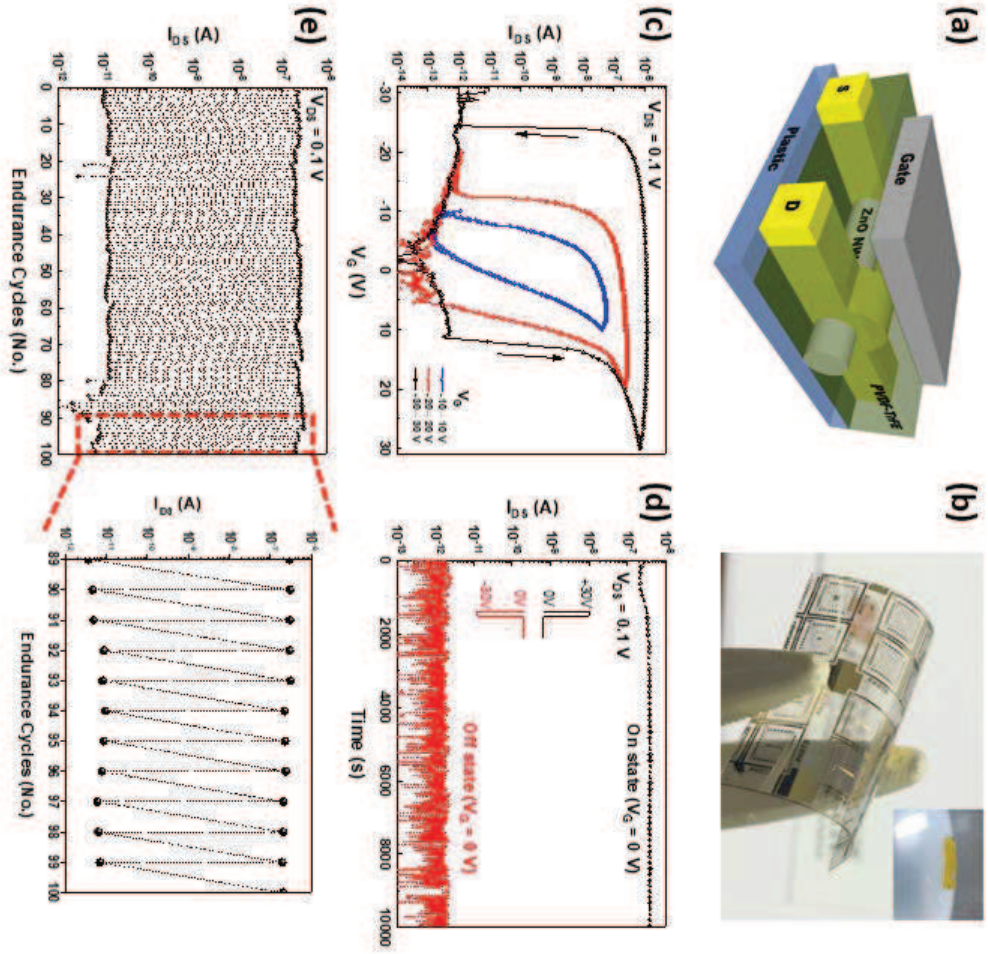

Figure 2.

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Figure 3.

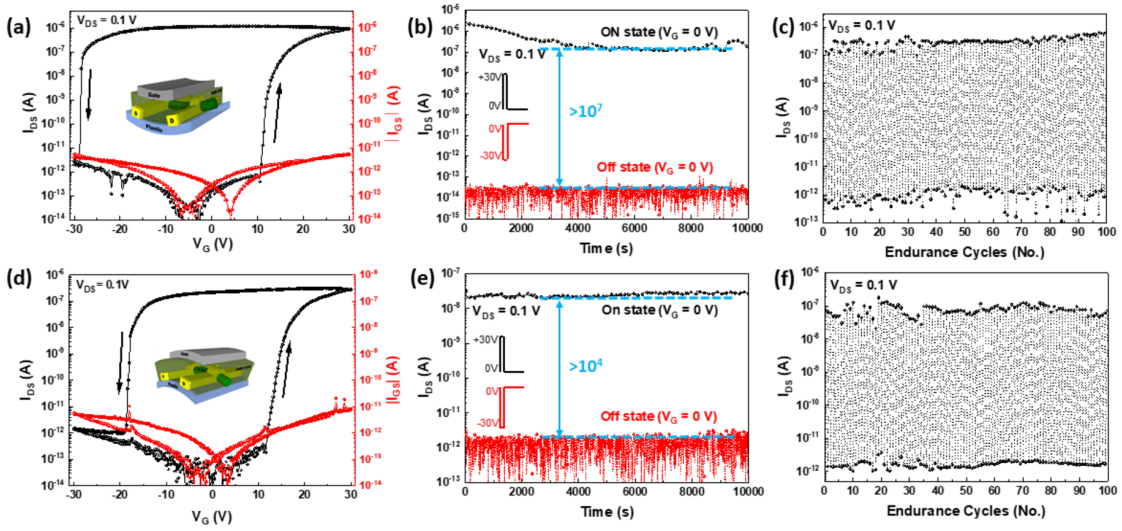

Figure 4. Chun *et al.*